

**WHAT IS CLAIMED IS:**

- 1           1.       An integrated circuit multiprocessor apparatus for processing a plurality of  
2 data packets, comprising:  
3           a plurality of processors;  
4           an interface circuit for receiving and transmitting a plurality of data packets;  
5           a memory comprising a plurality of descriptors, each of said plurality of  
6 descriptors comprising an ownership indication, a start of packet indication, an end of  
7 packet indication, a buffer length value and a buffer address for specifying a location of a  
8 buffer in memory for storing at least a portion of a data packet;  
9           a packet manager circuit coupled between the interface circuit and the memory to  
10 transfer data packets between the interface circuit and memory, wherein the packet  
11 manager circuit is configured to transfer a first data packet under control of at least a first  
12 descriptor and to transfer a second data packet under control of at least a second  
13 descriptor, wherein said packet manager is configured to write back to memory all  
14 descriptors associated with a data packet upon completion of the transfer of said data  
15 packet and said descriptors are written back in the order in which they are released.
- 1           2.       The apparatus recited in claim 1, wherein the each data packet is  
2 associated with a descriptor ring comprising a plurality of descriptors, each of the  
3 plurality of descriptors identifying a memory buffer in the memory for storing at least a  
4 portion of a data packet.
- 1           3.       The apparatus recited in claim 1, wherein the packet manager circuit  
2 comprises a packet manager input circuit coupled between the interface circuit and the  
3 memory to transfer data packets from the interface circuit to memory, wherein the packet  
4 manager input is configured to transfer a first data packet to memory only after the at  
5 least a first descriptor is read that has its ownership indication set.

1           4.       The apparatus recited in claim 1, wherein said packet manager is  
2 configured to reset the ownership indication in each descriptor after completing transfer  
3 of data under said descriptor.

1           5.       The apparatus recited in claim 1, wherein the at least a first descriptor  
2 comprises:  
3           a start descriptor having its start of packet indication set, where said start  
4 descriptor identifies a memory buffer where the start of the first data packet is stored; and  
5           a last descriptor having its end of packet indication set, where said last descriptor  
6 identifies a memory buffer where the end of the first data packet is stored.

1           6.       The apparatus recited in claim 5, wherein the at least a first descriptor  
2 comprises at least one middle descriptor having both its start of packet indication and end  
3 of packet indication reset.

1           7.       The apparatus recited in claim 1, wherein the at least a first descriptor has  
2 its start of packet indication and end of packet indication set.

1           8.       The apparatus recited in claim 1, further comprising a load balancing  
2 processor for distributing the plurality of data packets to the plurality of processors for  
3 processing by assigning a first consecutive group of the plurality of descriptors to a first  
4 processor and a second consecutive group of the plurality of descriptors to a second  
5 processor, wherein the first processor snoops on a last descriptor in the first consecutive  
6 group of descriptors for said first processor to detect when the last descriptor has its  
7 ownership indication reset by the packet manager circuit.

1           9.       The apparatus recited in claim 8, wherein the first processor processes at  
2 least a first claimed data packet by scanning back through the first consecutive group of  
3 descriptors, starting with the last descriptor having its ownership indication reset, to  
4 identify any descriptor having an end of packet indication set, and then scanning back  
5 further through the first consecutive group of descriptors to identify any packet start

6 descriptor having a start of packet indication set, said at least first claimed data packet  
7 comprising the packet start descriptor and the last descriptor.

1 10. The apparatus recited in claim 9, wherein the first processor processes a  
2 claimed data packet by further scanning back through the plurality of descriptors to  
3 identify a packet start descriptor if said packet start descriptor is not included in the first  
4 consecutive group of descriptors assigned to the first processor.

1 11. A system for controlling distribution of a plurality of data packets to a  
2 plurality of processors, said system comprising:  
3 a plurality of consecutive descriptor entries;  
4 a DMA controller for reading the plurality of consecutive descriptor entries;  
5 storing data packets in a plurality of buffers, each of the plurality of consecutive  
6 descriptor entries specifying a buffer for storing at least a portion of a data packet; and  
7 releasing ownership of the plurality of consecutive descriptor entries in order upon  
8 completing storage of a data packet;  
9 a plurality of processors, each processor configured to process packets; and  
10 an assignment processor for assigning a first group of descriptors from the  
11 plurality of consecutive descriptor entries to a first processor and for assigning a second  
12 group of descriptors from the plurality of consecutive descriptor entries to a second  
13 processor;  
14 where each processor in the plurality of processors is configured to spin on the  
15 final descriptor in its assigned group of descriptors and to process any packet comprising  
16 any EOP descriptors contained with its assigned group of descriptors along with any  
17 other descriptors associated with each EOP descriptor.

1 12. The system recited in claim 11, wherein each of said plurality of  
2 consecutive descriptor entries comprises an ownership indication, a start of packet  
3 indication, an end of packet indication, a buffer length value and a buffer address for  
4 specifying a location of a buffer in memory for storing at least a portion of a data packet.

1            13.    The system recited in claim 12, wherein an EOP descriptor comprises a  
2 descriptor entry having an end of packet indication set.

1            14.    The system recited in claim 11, wherein the descriptors associated with  
2 each EOP descriptor are determined by scanning back through the assigned group of  
3 descriptors to identify an SOP descriptor.

1            15.    The system recited in claim 11, wherein the descriptors associated with  
2 each EOP descriptor are determined by scanning back through the plurality of  
3 consecutive descriptor entries, starting with its assigned group of descriptors, to identify  
4 an SOP descriptor if said an SOP descriptor is not included in the assigned group of  
5 descriptors for said processor.

1            16.    The system recited in claim 12, wherein each processor in the plurality of  
2 processors determines the length of an assigned packet by summing the buffer length  
3 values for each descriptor associated with the assigned packet so as to support an  
4 unlimited packet size.

1            17.    A method comprising:  
2            creating and releasing a plurality of descriptors to a packet manager, said plurality  
3 of descriptors comprising a first descriptor group and a second descriptor group;  
4            assigning a first subset of the plurality of descriptors to a first processor and a  
5 second subset of the plurality of descriptors to a second processor;  
6            receiving a first packet in an interface circuit and transferring the first packet to at  
7 least a first memory buffer under control of the first descriptor group;  
8            receiving a second packet in the interface circuit and transferring the second  
9 packet to at least a second memory buffer under control of the second descriptor group;  
10           releasing the first descriptor group to software by writing the first descriptor  
11 group to memory;  
12           releasing the second descriptor group to software by writing the second descriptor  
13 group to memory; and

14           at each processor, identifying any EOP descriptor in the assigned subset of the  
15 plurality of descriptors and processing any descriptor associated with said EOP  
16 descriptor.

1           18.     The method recited in claim 17, wherein each processor identifies any  
2 EOP descriptor in the subset of the plurality of descriptors assigned to said processor by  
3 snooping on a last descriptor from the assigned subset of the plurality of descriptors and  
4 scanning back through said assigned subset of the plurality of descriptors to identify any  
5 EOP descriptor and any descriptor associated with said EOP descriptor.

1           19.     The method recited in claim 18, wherein any descriptor associated with  
2 said EOP descriptor comprises said identified EOP descriptor and SOP descriptor.

1           20.     The method of claim 17, wherein said first descriptor group comprises at  
2 least one descriptor, where said at least one descriptor comprises an ownership bit, a start  
3 of packet bit, an end of packet bit, a buffer length value and a buffer address for  
4 specifying a location of a buffer in memory for storing at least a portion of a data packet.

1           21.     The method of claim 17, wherein a processor identifies a first descriptor as  
2 an EOP descriptor by checking to see if an EOP bit is set in the first descriptor.

1           22.     The method of claim 17, wherein a processor identifies a first descriptor as  
2 an SOP descriptor by checking to see if an SOP bit is set in the first descriptor.

1           23.     The method of claim 17, wherein a processor determines that a first  
2 descriptor contains an entire packet by checking to see if both an SOP bit and an EOP  
3 bit are set in the first descriptor.